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Typical Implementation of VITERBI Decoder for efficient error detection and correction

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***Abstract*—** In the communication system, channel introduces noise and interference, which leads in distortion of transmitted signal due to which bit error may exists. To avoid this problem we proposed a Convolution encoder in the channel encoder and Viterbi decoder in the channel decoder which has error correcting capability. This paper deals with the implementation of Convolution Encoder with 2 bit code rate so it generates two bits for each bit of input data. Modified Viterbi decoder is designed to decode this encoded data without error because it has main advantage that it has the capability to detect errors and correct them effectively. We can design one particular input pattern and generate the encoded pattern using our designed encoder and it can be decoded by our Viterbi decoder without any error. Here we implemented our design using 2 bit and ½ bit code rates. Viterbi decoding for Convolutional Codes is presented here as an efficient system for reliable communication over limited noisy digital communication channels. In future it may be further extended to more bit code rates to improve its performance with less complexity.

Keywords: *Convolution encoder, Viterbi Decoder, Path metric, Trellis diagram.*

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I. INTRODUCTION

Communications is the study of the transmission of various data through different systems. We can transfer the information from one region to another without any loss of the data. Transmitter side source, channel encoder in that way receiver side channel, source decoders are important to have better communication.

II. CONVOLUTION ENCODER

Channel coding is the process of adding the redundant information. Convolution coding and block coding are the two main forms of channel coding. This paper deals with the implementation of convolution encoder constraint length of K=2 and with code rate=1/2.

A. Encoder design

In this paper we have designed convolution encoder in the way in which that the output bits can be decoded without error. Here each input bit of data, two output bits are generated with the logic shown below. The input bits are applied serially, to m0 which represents present state, m1 and m2 represents next state. As there are two bits to represent next state, there are 4 possible combinations here is called states of the system.

B. Functional description

Here input bit changes the state of encoder to generate encode data. There are two possible next states for each present state depending on the sequence. Here we have considered 3 bit register to store bits and convolute them to generate encoded data. At every clock cycle edge the input bit is loaded, operated and then shifted. The output bits pair for each input bit is transmitted to receiver, where there is a possibility of noise interference.

The convolution encoder functional block and state diagrams are shown below.

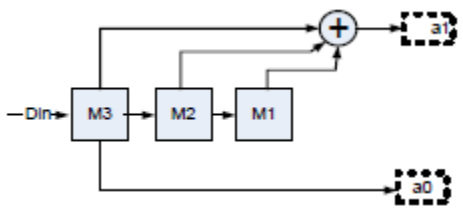

Fig. 1. Convolution encoder functional block

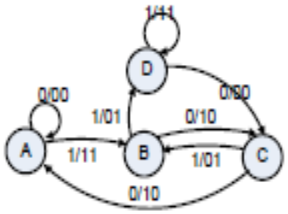

Fig. 2. State diagram of convolution encoder

The diagrammatic representation of our designed convolution encoder is shown below:

Here Output 1=a0= m (3)
Output 2=a1=m (3) XOR m (2) XOR m (1)

Table. 1. Convolution Encoder function table

Input Data M0	Machine State Present State			Output		Machine State Next State
	M2	M1	State	O2	O1	
0	0	0	A	0	0	A
1				1	1	B
0	0	1	B	1	0	C
1				0	1	D
0	1	0	C	1	0	A
1				0	1	B
0	1	1	D	0	0	C
1				1	1	D

Transmitted data=1001110
Encoded data=00110111101011

Convolution encoder takes input data M0, encoded this and passes through the channel. Then this encoded data is decoded by viterbi decoder and correct its error.

III. VITERBI DECODER

Viterbi decoder is designed as channel decoder in the communication system to detect the error. Here viterbi decoder is designed also for correcting the encoded date by convolution encoder at transmitter side. It receives data from channel which was sent by convolution encoder.

A. Functional block:

In this work Viterbi decoder has one machine and two sub machines of functional block diagram is as shown below:

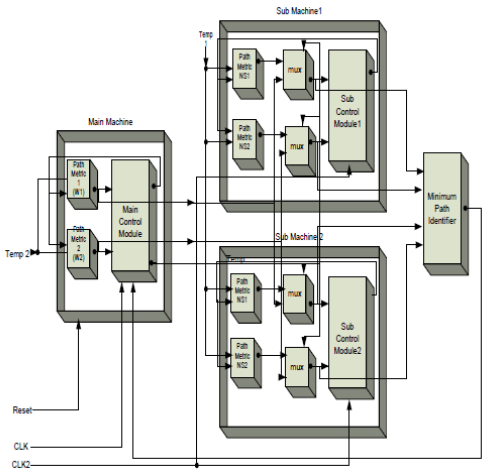

Fig. 3. Block diagram of VITERBI decoder

B. Functional behavior of VITERBI decoder:

Here first main machine responds for first two bits of encoded data by calculating path metrics and branch metrics in all cases mean while both sub machines calculates the path metrics using present loaded data bits and it can be compared. It can be done before main machine completes its work because of its double clock rate. When path metrics of main machine is same then this data can be used otherwise it will be neglected. The flowchart of our designed viterbi decoder process flow is as shown below.

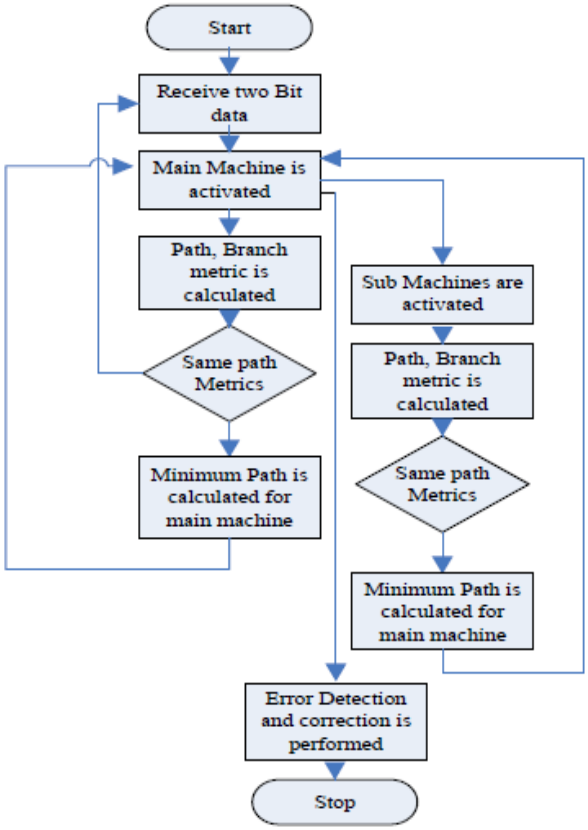

Fig. 4 Flow chart of VITREBI decoder

The finite state machine diagram of our designed viterbi decoder is as shown below.

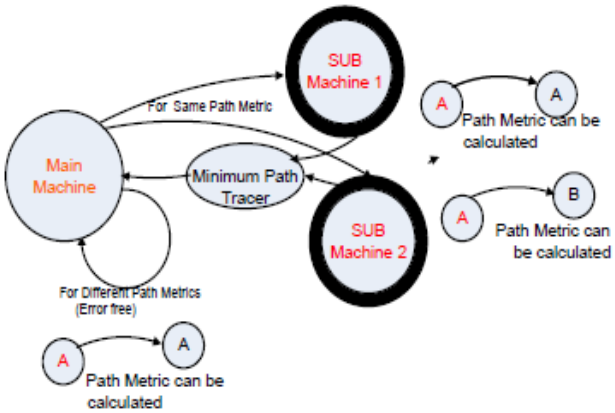

Fig. 5. State diagram of viterbi decoder

Condition for the next state is given the table shown below for all cases when main machine is in all states. Here in this table all sub machines states and possible next states for all possible weights are also represented below.

Table .2. Convolution Encoder function table

Decoder Main machine Present State	Condition For Next State				Decoder Main Machine Next State
	Main Machine Path metric (W1,W2)	Sub Machines M1	Sub Machines M2	PT generated by minimum Path tracer	
A	W1<W2	A	A	-	A
	W1>W2	B	B	-	B
	W1=W2	A	B	0	A
		A	B	1	B
B	W1<W2	C	C	-	C
	W1>W2	D	D	-	D
	W1=W2	C	D	0	C
		C	D	1	D
C	W1<W2	A	A	-	A
	W1>W2	B	B	-	B
	W1=W2	A	B	0	A
		A	B	1	B
D	W1<W2	C	C	-	C
	W1>W2	D	D	-	D
	W1=W2	C	D	0	C
		C	D	1	D

The Trellis diagram of our designed Viterbi decoder process flow is as shown below.

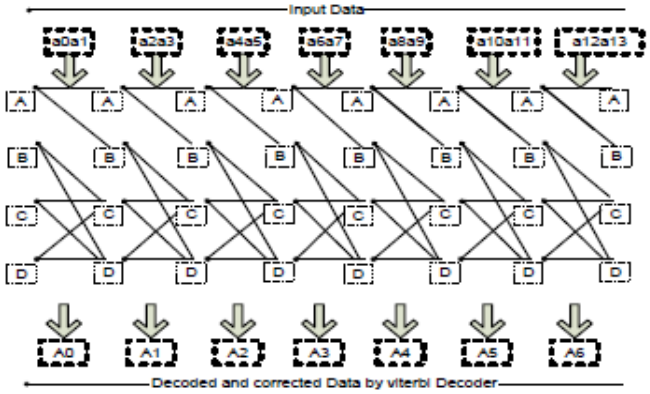

Fig. 6. Trellis Diagram for Viterbi decoder

For receiving pairs of input data at each state decoder generates 1-bit data as decoded output which is nothing but our actual input message.

IV. SIMULATION RESULTS AND COMPARISONS

Convolution encoder and viterbi decoder functional simulation results:

Consider a bit pattern "1001110" to transmit in digital network. Convolution encoder generates 2 bits for each bit and this coded data transmit over channel.

Consider received data with error is given as 0111111110101. This data will be decoded by Viterbi decoder by taking 2-bits as single input and produces one bit output each combination.

Decoded data =1001110

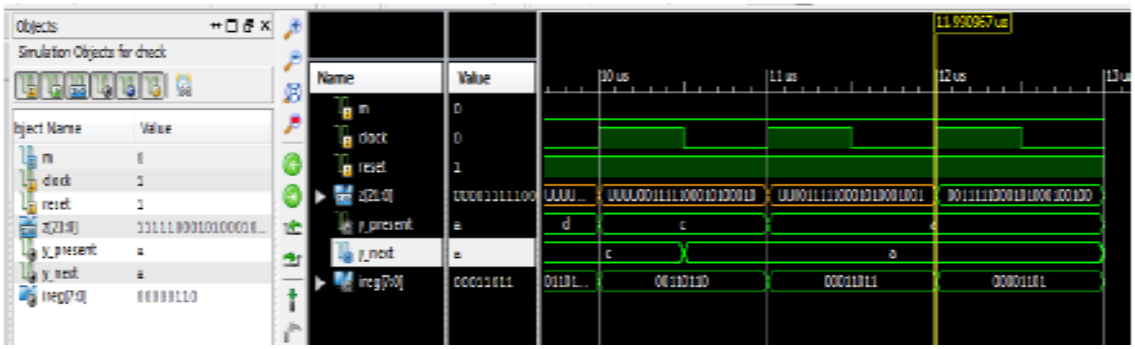

Fig. 7. Simulation waveforms of 2-bit coded convolution encoder

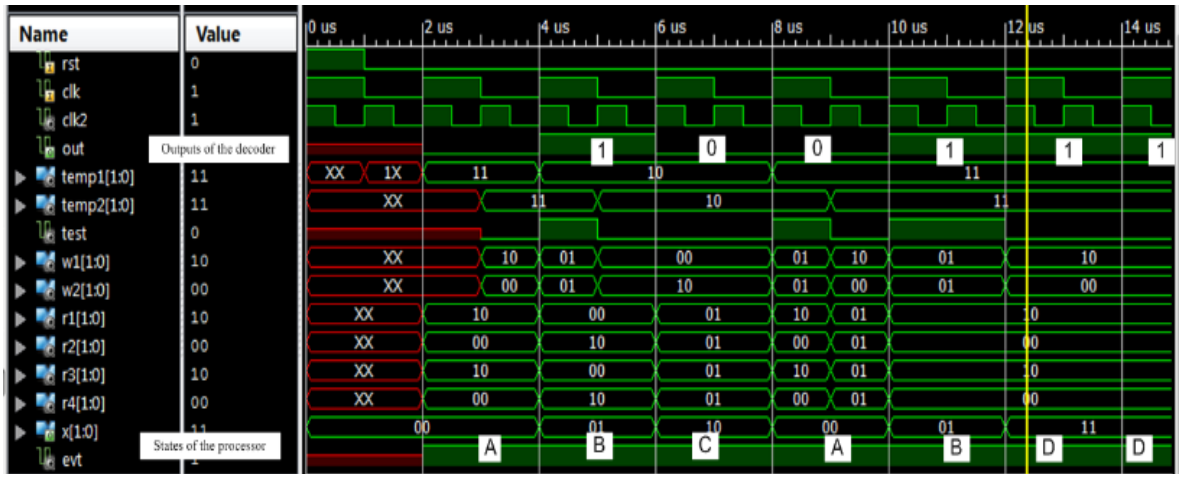

Fig.8. Simulation results of entire Viterbi decoder

Implementation results:

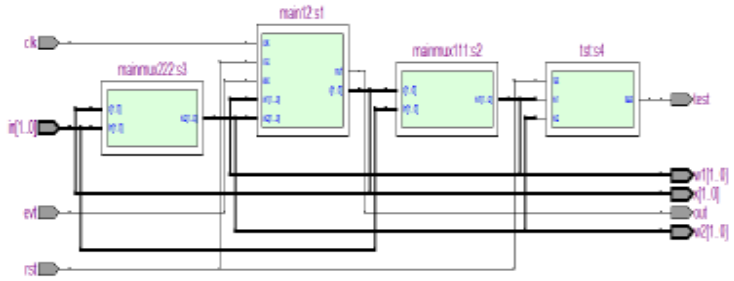

Fig. 9.RTL Schematic view of first sub machine

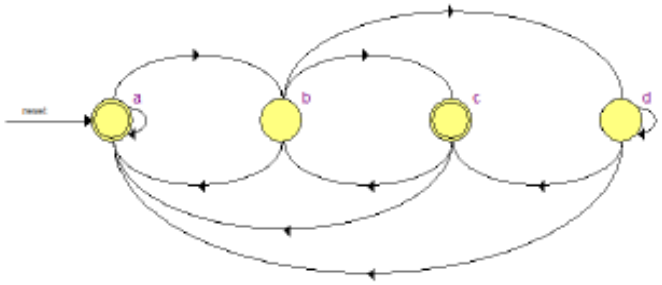

Fig. 10. State machine view of main machine

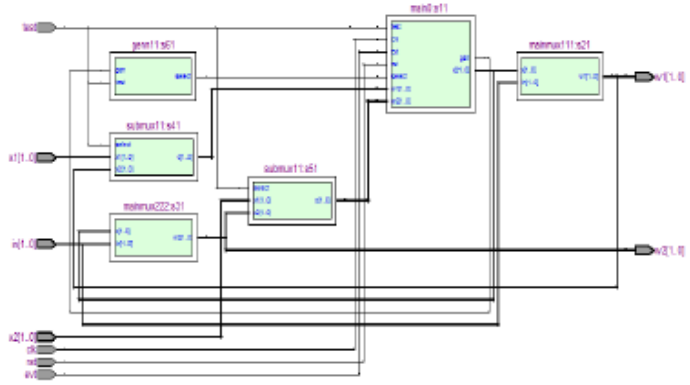

Fig. 11. RTL schematic view of sub machine

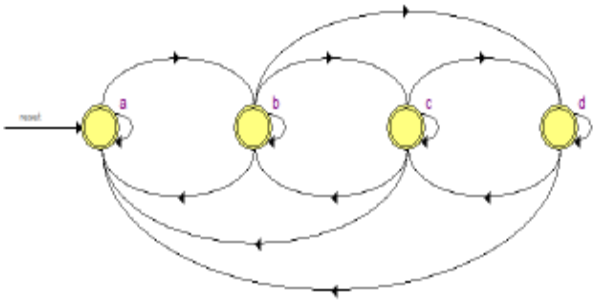

Fig. 12 State machine view of sub machine

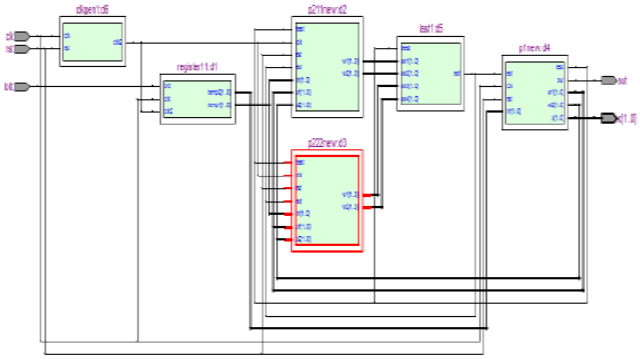

Fig. 13 RTL schematic view of entire Viterbi decoder

V. CONCLUSION

Here in this paper Convolution Encoder is designed with 2 bit code rate because it can generate two bits from each bit of input data according to our specified output functions. A modified Viterbi decoder is also designed with single clock pulse for main machine and another two sub machines which are running at double clock speed. Here advantage with this modified circuit sub machines is that they can trace out the minimum path before main machine calculating its metric avoid delay. Also another main advantage of our viterbi decoder is that it is having the capability to detect errors and correct them effectively in the communication system. Here our design is implemented using 2 bit and ½ bit code rates. In future this can be further extended to more bit code rates to improve its performance with extra machines.

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