IOSR Journal of Engineering (IOSRJEN) **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
Vol. 08, Issue 7 (July. 2018), ||V (VI) || 01-06

FPGA Realization of Autonomous Chaotic Generator using RK4-based Algorithm

[1]Subodh Kumar Pandey, [2]Sanjeev Kumar Gupta
[1]Research Scholar, Department of Electronics& Communication Engineering
Rabindranath Tagore University, Chiklod Road Raisen-464993 (M.P.)
[2]Professor and Dean Department of Electronics& Communication Engineering
Rabindranath Tagore University, Chiklod Road, Raisen-464993 (M.P.)

Abstract–Now a days chaotic systems have an important role in secure communication and cryptography. As FPGA implementation have certain advantages over analog one, different chaotic system like chaotic oscillator, True random number generators and chaotic systems used in image processing, optical circuits for secure communications were successfully realized in FPGA. This paper presents FPGA implementation of Autonomous Pandey-Baghel-Singh chaotic signal generators using RK 4 algorithm. Numerical solution of Differential equation system is obtained and coded in Verilog and tested with Xilinx vivado 17.3 design suite in Artix-7 Nexus 4 DDR and Basys 3. Performance of the FPGA based chaotic generators is analyzed using 10^6 data sets with the maximum operating frequency achieved up to 359.71MHz.

Key Words - *Chaotic Generators, RK 4 algorithm, FPGA*

Date of Submission: 13-07-2018 Date of acceptance: 29-07-2018

I. INTRODUCTION

Chaos generator is a fundamental block of any chaos based system. Basically chaos based system are used in secure communication and cryptography. Recently implementation of FPGA based real time chaotic oscillator using different numerical algorithm were presented and it was shown that the processing speed of FPGA is much higher due to parallel processing capabilities. Hence it may be interesting to see the performance of FPGA based different chaotic systems as the analog based design of chaos based generators is sensitive to initial conditions and acquires a large chip area. To avoid these problems Digital based design chaotic systems using FPGA can be implemented as FPGA implementation is more flexible architecture and have low cost test cycle and found more useful in chaos based engineering applications [1-7].

In II section of the paper presented the Pandey-Baghel-Singh Chaos System (PBSCS) is described along with their x, y and z signals and their attractors [8]. In the III section the mathematical models of PBSCS is numerically obtained with RK 4 algorithm and FPGA model of PBSCS is introduced. In the IV section simulation results has been presented and analyzed. In section V conclusion is given.

II. INTRODUCTION TO PANDEY- BAGHEL-SINGH CHAOS SYSTEM

Pandey-Baghel-Singh Chaos System (PBSCS) is defined by the set of differential equation (1)

$$\begin{aligned} \dot{x} &= y \\ \dot{y} &= z \\ \dot{z} &= -ax - by - cz - x^2 \end{aligned} \tag{1}$$

In the system two equilibrium points as (0, 0, 0) and (-1, 0, 0) were shown for the constants a = 1, b = 1.1, and c = 0.4.The equilibrium point (0, 0, 0) have the Eigen values -0.745, 0.162+j1.147and 0.162-j1.147. For the equilibrium point (-1, 0, 0) the Eigen values shown are 0.589, -0.504+j1.20, and -0.504-j1.20. The initial condition for the system is taken for x = 0.1, y = 0 and z = 0.The time domain representation of x, y and z waveform are given in Fig.1 and attractors generated are given in Fig. 2 (a-c).

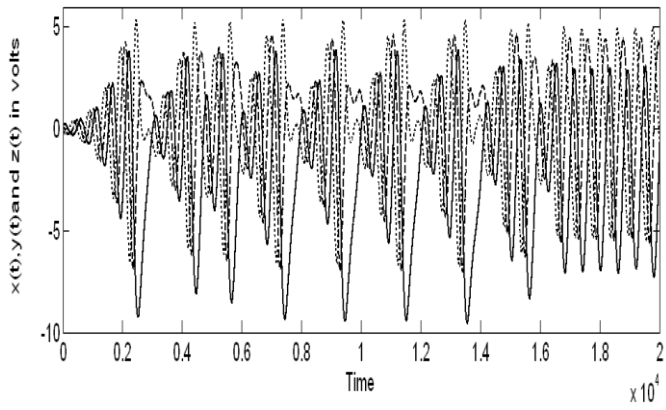
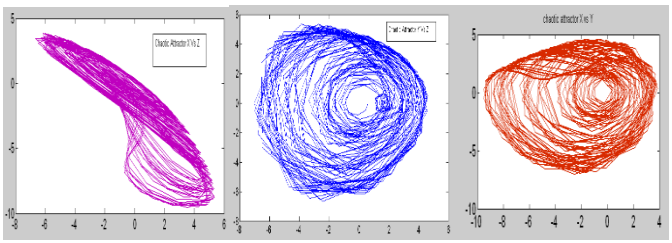


Fig. 1: Time domain representation of x, y and z signals of PBSCS.



(a) (b) (c)

Fig.2: (a) x-y attractor, (b) y-z attractor, (c) x-z attractor

III. RK 4 BASED NUMERICAL MODEL OF PBSCS AND ITS FPGA IMPLEMENTATION

For FPGA implementation of the system the numerical model is obtained using RK 4algorithm and coded in Verilog.

A. Numerical model using RK 4 algorithm

To construct the mathematical model of the PBSCS using RK4 algorithm, the system equation are represented as a function of $f, g \; and \; \delta$ as equation

$$\begin{aligned} \dot{x} &= f(t,x,y,z) = y \\ \dot{y} &= g(t,x,y,z) = z \\ \dot{z} &= \delta(t,x,y,z) = -ax - by - cz - x^2 \end{aligned} \tag{2}$$

With respect to above equation the mathematical model of the system using RK4 algorithm is given in equation (3). The parameter $K, \lambda \; and \; \xi$ defined as the coefficients of the first, second and third equations respectively given in equation (2) and are placed in equation (3) to calculate the $x(k+1),\ y(k+1) \; and \; z(k+1)$ which are the values of the system after h steps. The values $x(k+1),\ y(k+1) \; and \; z(k+1)$are the output of the system after each interval which are used as initial conditions of the algorithm to calculate the values for the next cycle.

$$\begin{aligned} x(n+1) &= x(n) + \frac{1}{6}h[k_1(n) + 2k_2(n) + 2k_3(n) + k_4(n)] \\ y(n+1) &= y(n) + \frac{1}{6}h[\lambda_1(n) + 2\lambda_2(n) + 2\lambda_3(n) + \lambda_4(n)] \\ z(n+1) &= z(n) + \frac{1}{6}h[\xi_1(n) + 2\xi_2(n) + 2\xi_3(n) + \xi_4(n)] \end{aligned} \tag{3}$$

$$\begin{aligned} k_1 &= f[x(n), y(n), z(n)] \\ \lambda_1 &= g[x(n), y(n), z(n)] \\ \xi_1 &= \delta[x(n), y(n), z(n)] \\ k_2 &= f[x(n) + \frac{1}{2}hk_1.y(n) + \frac{1}{2}h\lambda_1.z(n) + \frac{1}{2}h\xi_1] \\ \lambda_2 &= g[x(n) + \frac{1}{2}hk_1.y(n) + \frac{1}{2}h\lambda_1.z(n) + \frac{1}{2}h\xi_1] \end{aligned}$$

$$\xi_2 = \delta[x(n) + \frac{1}{2}hk_1.y(n) + \frac{1}{2}h\lambda_1.z(n) + \frac{1}{2}h\xi_1]$$
$$k_3 = f[x(n) + \tfrac{1}{2}hk_2.y(n) + \tfrac{1}{2}h\lambda_2.z(n) + \tfrac{1}{2}h\xi_2] \quad (4)$$
$$\lambda_3 = g[x(n) + \frac{1}{2}hk_2.y(n) + \frac{1}{2}h\lambda_2.z(n) + \frac{1}{2}h\xi_2]$$
$$\xi_3 = \delta[x(n) + \frac{1}{2}hk_2.y(n) + \frac{1}{2}h\lambda_2.z(n) + \frac{1}{2}h\xi_2]$$
$$k_4 = f[x(n) + hk_3y(n) + h\lambda_3z(n) + h\xi_3]$$
$$\lambda_4 = g[x(n) + hk_3y(n) + h\lambda_3z(n) + h\xi_3]$$
$$\xi_4 = \delta[x(n) + hk_3y(n) + h\lambda_3z(n) + h\xi_3]$$

B. FPGA Implementation of Autonomous Chaotic Generator based on RK 4 algorithm

The PBSCS has been modeled using RK 4 algorithm and implemented with 32- bit IEEE 754-1985 standard on FPGA. Mathematical modeling is done in Verilog using Vivado design suite. Top-level diagram of RK 4based units have been shown in Fig. 3. A 32-bit input has been used and initial conditions are set in the beginning phase. The 32-bit signal are used as input parameter. There is three 32-bit output signals (Xn_out), (Yn_out) and (Zn_out) and ready signal is taken as one bit control signals for the proposed RK 4 based chaotic generators.

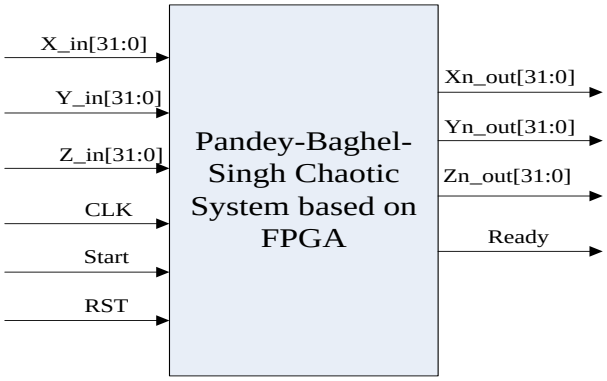


Fig.3 Top level diagram of PBS Chaotic System based on FPGA

In Fig. 4 the 2nd level block diagram of the RK 4 based chaotic generator is presented. It have one multiplexer and a chaotic generator unit which is FPGA based. The multiplexer is used to provide initial condition signals. For successive operation it is provided by the output signals. When enable is at logic high, the output generates chaotic signal.

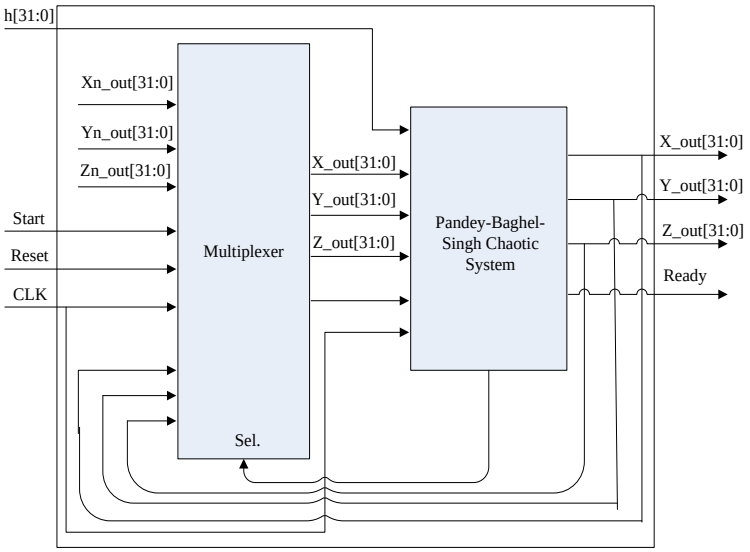


Fig.4 2ndlevel diagram of PBSCS based on FPGA

The3rdlevel block diagram of the RK 4 based chaotic generator is given in Fig. 5. The proposed chaotic generator consist of multiplexer, K_s units, Y_s block and filter stage. K_s units calculate $k_s, \lambda_s \; and \; \xi_s$ where s varies between1 to 4. The $x(k+1), \;\; y(k+1) \;\; and \;\; z(k+1)$given in equation (3)are calculated at Y_s block. The first value is generated after 142 clock Pulses and a feedback system is to be employed so that output is feedback to MUX after 142 clock pulses to generate next cycle. Filter unit stops undesired signal to reach output if generator does not generate any result.

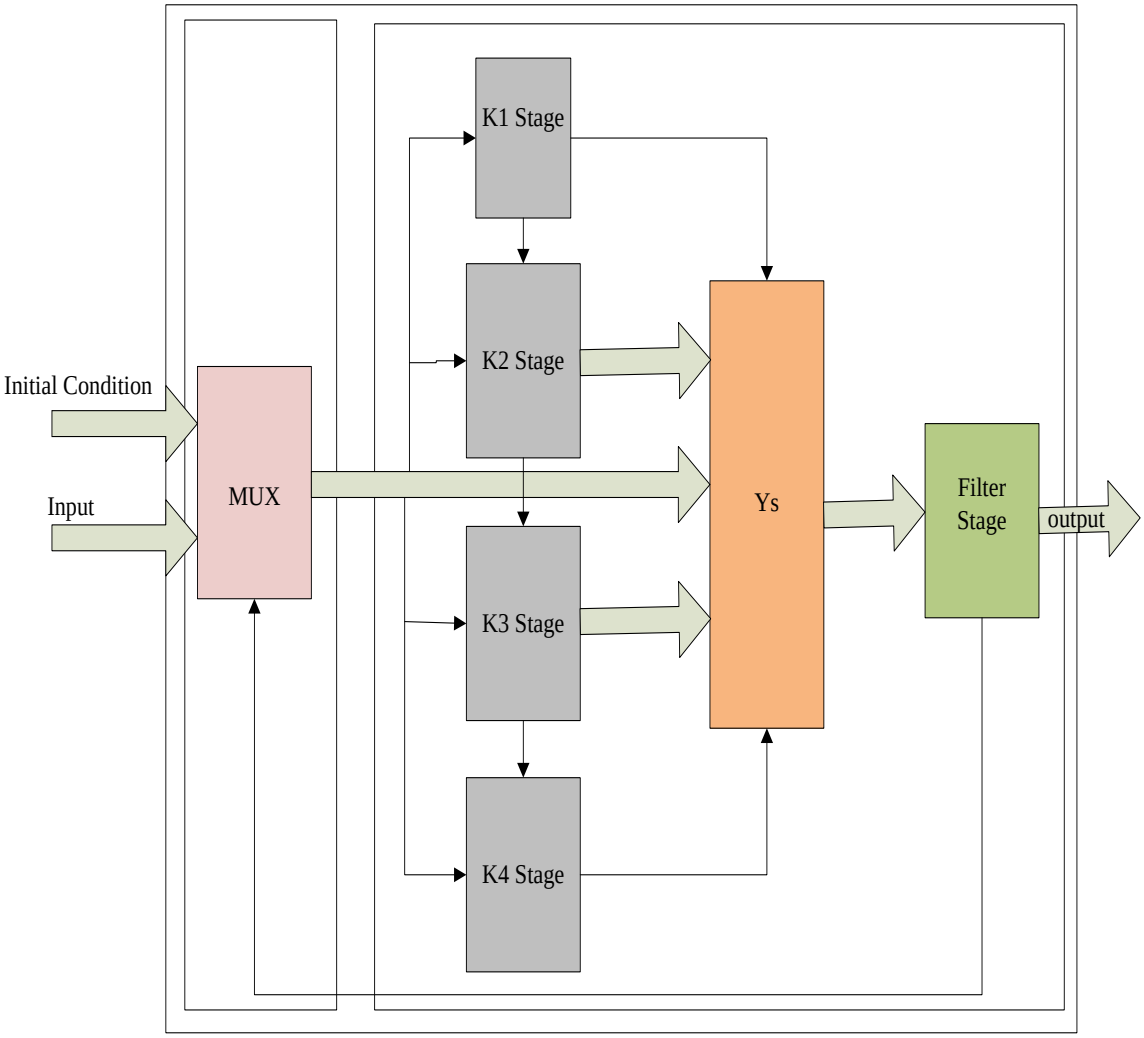


Fig. 5 3rdLevel diagram of RK 4 based PBSCS Generator Unit

IV. SIMULATION RESULTS OF PBS CHAOTIC GENERATOR

The RK 4 algorithm based PBS Chaotic generator have been synthesized for the Nexus 4 DDR XC7A100TCSG-1 (Artix7) and Basys3 (Artix7) from the Xilinx Vivado v.2017.3 design suite. FPGA chip related Parameters and clock speed of the system have been analysed. The simulation results of the RK 4 based PBSCS is presented in the Fig. 6 and Fig. 7. The results are analysed in hexadecimal format. The attracter of the system is generated by the data set using MATLAB are given in fig. 8 (a-c). The parameter related to design for Nexus 4 DDR XC7A100TCSG-1 (Artix7) and Basys3 (Artix7) which are obtained for the RK 4 algorithm is given in table 1. For the optimize result the clock period of 2.78 ns is set and which corresponds to maximum frequency of 359.71 MHz the number of LUT's and registers used are 2637 and 4692 respectively.

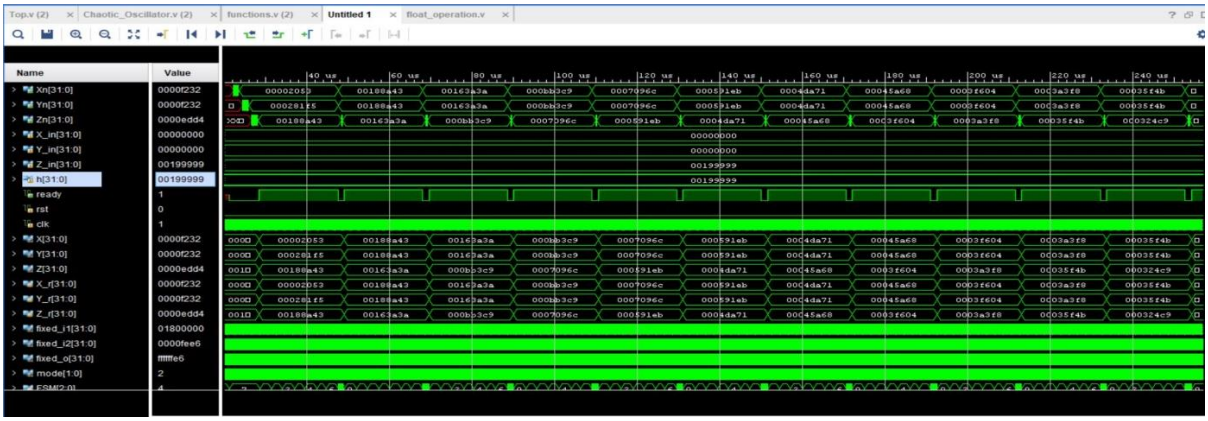


Fig.6 Timing simulation results of RK 4 based PBSCS obtained from Xilinx Vivado 17.3

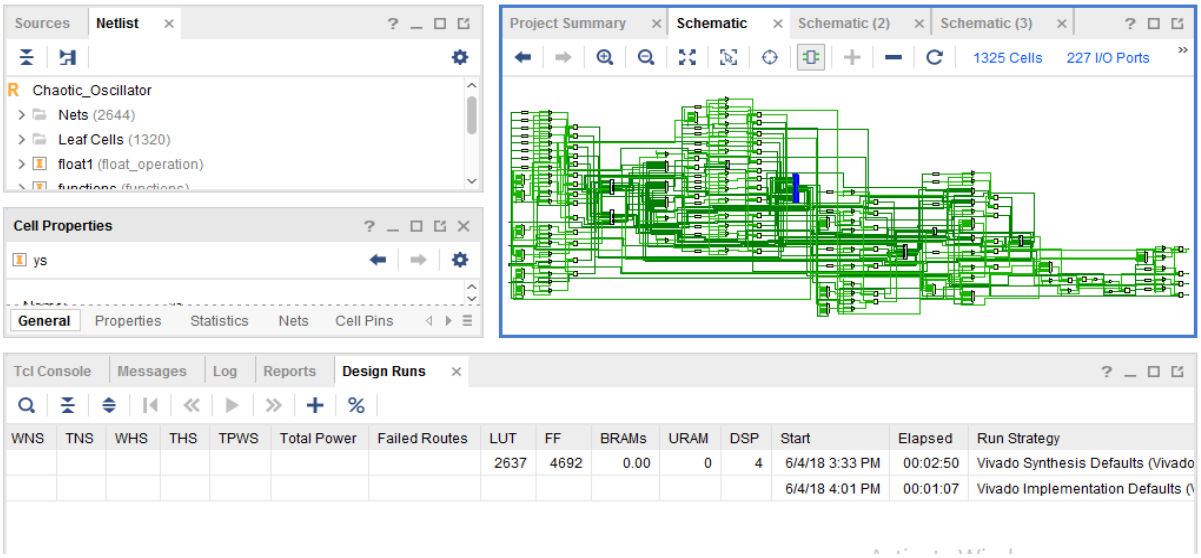
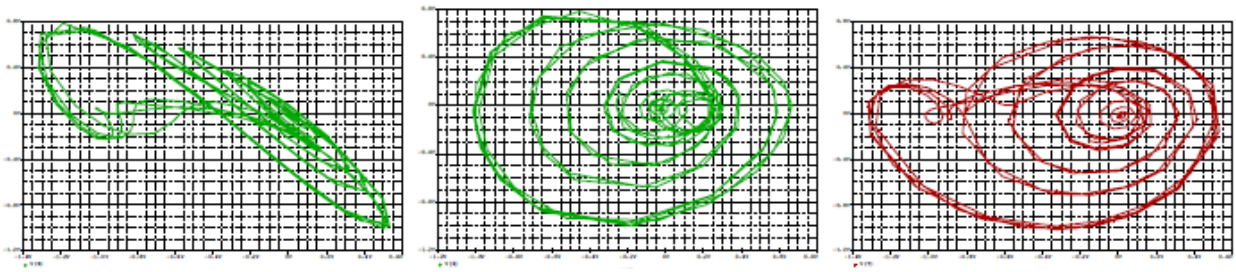


Fig.7 Simulation result of PBSCS on Vivado 17.3



(a) (b) (c)

Fig. 8 (a) x-y attractor, (b) y-z attractor, (c) x-z attractor

Maximum frequency (MHz)	359.71
No. of DSP	4
Number of 4 input LUTs	2637
Number of bonded IOBs	32
Number of Slice Flip Flops	4692
Total On-chip Power(W)	0.179

Table 1: Final report of the resources consumption

V. CONCLUSION

The RK 4 algorithm based PBS Chaotic generator have been synthesized using the Nexus 4 DDR XC7A100TCSG-1 (Artix7) and Basys3 (Artix7) from the Xilinx Vivado v.2017.3 design suite. For the optimize result the clock period is set to 2.78 ns which uses2637 LUT's and 4692 registers and the maximum frequency achieved is 359.71 MHz. The attractors generated for the FPGA based design are similar to PBSCS designed on analog platform.

REFERENCES

[1]. Ismail K., A. Tuaran O, Ihsan Pehlivan, "Implementation of FPGA-based real time novel chaotic oscillator", Nonlinear dynamics (2014) ; pp. 49-59.
[2]. Murat Tunaa, Can Bülent Fidan, "Electronic circuit design, implementation and FPGA-basedrealization of a new 3D chaotic system with singleequilibrium point", Optic ElsevierOptik (2016) pp. 11786–11799.
[3]. S. Banerjee, J. Kurths, "Chaos and cryptography: a new dimension in secure communications", Eur. Phys. J. Spec. Top. , (2014) pp. 1441–1445.
[4]. I. Koyuncu, A.T. Ozcerit, I. Pehlivan, "An analog circuit design and FPGA-based implementation of the Burke-Shaw chaotic system", Optoelectron. Adv.Mater. Rapid Commun. (2013) pp. 635–638.
[5]. L. Merah, A. Ali-pacha, N.H. Said, "A pseudo random number generator based on the chaotic system of Chua's circuit and its real time", FPGA Implementation (2013) pp. 2719–2734.
[6]. S. C¸ ic¸ ek, A. Ferikog˘lu, I˙. Pehlivan, "A new 3D chaotic system: dynamical analysis, electronic circuit design, active control synchronization and chaotic masking communication application", Optik – Int. J. Light Electron Opt. (2016) pp. 4024–4030.
[7]. M. Tuna, I. Koyuncu, C.B. Fidan, I. Pehlivan, "Real time implementation of a novel chaotic generator on FPGA", in: 2015 23rd Signal Processing andCommunications Applications Conference (SIU), IEEE, 2015, pp. 698–701.
[8]. Alpana Pandey, R. K. Baghel, R.P. Singh, "Analysis and Circuit Realization of a NewAutonomous Chaotic System", International Journal of Electronics and Communication Engineering.ISSN 0974-2166 Volume 5, Number 4 (2012), pp. 487-495

Subodh Kumar Pandey "FPGA Realization of Autonomous Chaotic Generator using RK4-based Algorithm." IOSR Journal of Engineering (IOSRJEN), vol. 08, no. 7, 2018, pp. 01-06.