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Implementation of Novel Approach LFSR Architecture for Power Optimized Applications

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Abstract: The major focused areas in VLSI are area, chip cost and its power. The switching activity is very high in generally during test mode due to continuous changing of data because the test patterns are applied randomly. So to reduce the consumption of power the switching activity has to be reduced. In the market now a day, the handy devices are very popular and its marketing is done only if it consumes less power.
A novel low power pattern generation method is implemented by means of a modified LFSR which can carry out fault analysis and diminish the circuit power by introducing three intermediate vectored patterns during the test mode. The main reason to introduce these test vectored patters is to reduce the activities of transitions of the primary inputs which obviously reduce the activity of switching pattern. So by this way the total switching during the test mode reduces. Obviously the consumption of power is automatically diminishes. By taking the c17 circuit as benchmark, the proposed design is tested for the fault coverage.

Keywords: FAULT COVERAGE, LFSR, C17 BENCHMARK.

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I. INTRODUCTION

From so many years ago the patterns which are using for testing the circuits are being generated by the conventional methodology. These methodologies included counters, LFSR's and some sequential generators. LFSR's are a series of registers which is having feedback taps whose tap values can be obtained based on the polynomial. The value which is used initially to generate the remaining patterns are termed as seed value. By using the clock pulse which is generated externally is the only input which is applied to pattern generator to generate the sequence of patterns. Based on the input vectors applied the chip switching activity consumes the power. If the correlation between the vectors is more then the power consumption is very less. If it is less obviously the consumption became more. So to reduce the consumption the vectors correlation should be improved. A new algorithm is proposed to perform the action which should increase the correlation between the consecutive vectors.

II. TESTING SCHEMES

Now a days power consumption is the major problem to design on SOC (system on chip) and its test also. In CMOS technology the power consumption may be dynamic or static. The static power consumption are very less compared to dynamic power consumption, those are occurred due to leakages of power. The dynamic power consumption are occurred due to the reason of switching of nodes from 1 to0 or 1to 1,it means on ,off condition of switches ,it consumes more power .And high power consumed load capacitance changes and current flow in short circuits. In any system consumes more power active mode compared to normal mode. If the interaction between two successive vectors is high, then the power consumption also decreases. If interrelationship is low then increases the power consumption, i.e to increase the relationship between two successive vectors we have to give some amount power. If we applying switching activity between two successive vectors its consumes less power. When we applying switching activity between non interrelations between consecutive vectors it consumes more energy to set interrelationship between that two vectors**.**

III. BIST ARCHITECTURE

A typical BIST architecture consists of Test pattern generator, Test response analyzer and control unit whose architecture is shown below.

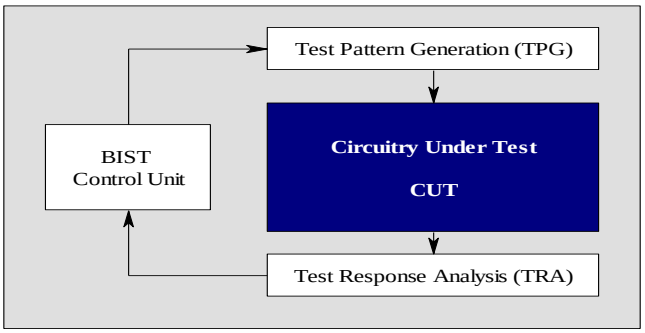

Fig 3.1 Test Pattern Generator

For the circuit under test the test patterns has to be applied which was generated.This may be processor or committed circuit. This test pattern generator is either a random one or it may be deterministic. In this paper an LFSR is using as a random no generator.

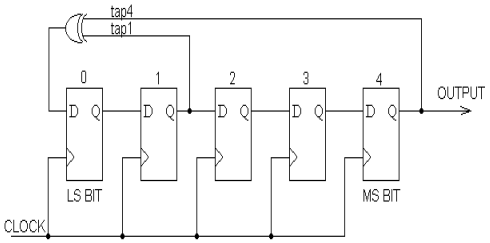

Fig 3.2 LFSR architecture

For the circuit the tapping bits may be any one which is purely based on the application which should be realized. But as the taping values are changed obviously the output which was generated from the LFSR is also changes. At the same time the lfsr output is also depending on the seed value which was taken. Seed value is nothing but the value which is taken as initial value to generate the patterns.

IV. LOW TRANSITION PATTERN GENERATION

To improve the traditional LFSR circuit we are using low power linear feedback shift register, here inserting the injected circuit to the traditional LFSR circuit .In this technique inserting the three intermediate vectors for test pattern generation. The below figure shows that LP_LFSR the circuit containing 9 Flip-flop for transmitting data bits. here size transmitting bit data is 8bits.The total bits dividing into two separate vectors ,each vector containing 4 bits.

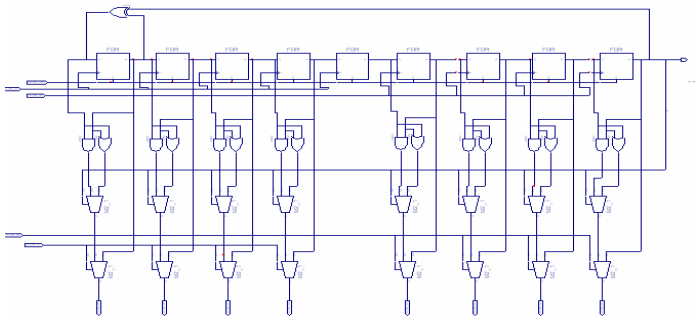

Fig 4.1 LP-LFSR

TheT1,T2 are test pattern generators and Ta, Tb and Tc are intermediate test pattern generators .If the initial data is 00101101.The first step is for generating T1.In this step first vector is in active i.e clock is enabling. the first 3 bits of data is shifted to right i.e 001. The last shaded flip flop is filled with first bit of first half vector ,which is stored in first flip flop,and last bit of second vector ,which is stored in last flip flop are

given to xor circuit i.e 1 xor 1 =0 then last bit filled with 0 i.e 0001.And the second vector is in ideal mode ,disabled with clock. Then previous output is propagated to the output .Then the out T1is 00011101. The next step is for generating Ta, Tb and Tc (intermediate vectors)we are using T1=00011101.For generating Ta, according to below algorithm first half vector is ideal I.e clock is disabling ,then the previous output is propagated to the output then 0001 is transmitted to output. And second half is active clock is enabling first three bits are shifted to right i.e110 and the last shaded flip-flop filled with 0(1 xor 1=0).And after compare two half vectors by using xor gate and send the output to the second half vector 0111(0 xor 0=0,0 xor 1 =1,0 xor 1=0 and 1 xor 0=1).The output of Ta=00010111.

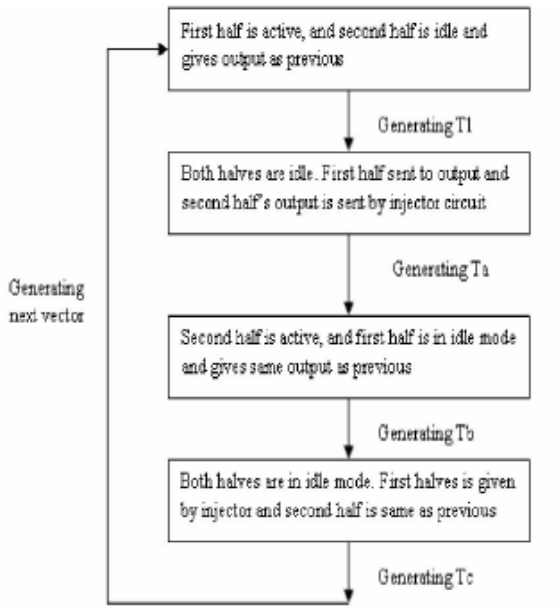

Fig 4.2 Proposed algorithm for low power LFSR

After we generating Tb by using first intermediate vector Tb. In this case according to above LP_LFSR algorithm first of is ideal ,disable to the clock signal in this case previous output send to the present output i.e 0001.And second half vector is active, clock is enabled to the circuit .The first three bits are shifted to right i.e 011.The last shaded flip flop is filled with 1,which is made up of first bit of first half vector, which is stored in first flip flop and last bit of second vector ,which is stored in last flip flop are given to xor gate i.e 1 xor 0=1.Then the propagation output of second intermediate pattern is Tb=00011011. Generating of Tc according to above algorithm both halves of vectors are ideal.If first half vector is ideal then previous output is sent to the present output i.e 0001 is the output of first half vector. And also second half vector is ideal then previous output send to the output i.e 1011.And the first half is connected to the injected circuit .In this state outputs of both halves compared to each other. Here xor logic circuit used for comparing module then 0 xor 1=1,0 xor 0=0,0 xor 1=1and 1 xor1=0.Then the output is 1010.The final output of Tc is 10101011. All test patterns are generated by using low power linear feedback shift registers .For generating T2 test pattern same as the T1 test pattern. In T2 test pattern generation second half vector is ideal ,disable to clock signal, in this case previous input is propagated to present output. And first half vector is active, i.e enable to clock signal. In this state last three bits are shifted to right i.e the first output bits are 101.And last shaded flip flop is filled with 1,which is come from first bit of first half vector ,which is stored iv first flip flop of first vector and last bit of second vector ,which is stored in 4 th flip flop of second vector are connected to xor logic(0 xor 1 =1). Then the out put first half vector is 1101.

The output of second pattern generator is T2=11011011.In the proposed LP_LFSR test patterns are generated continuously until all patterns are generated, by using low power linear feedback shift registers. And all patterns are applied to the C17 bench mark circuit. Here the comparator is used as the bench mark circuit .To apply the values to the comparator, it compares the values of tested circuit with the original circuit. And it detect the fault in tested integrated circuit is correct or not.

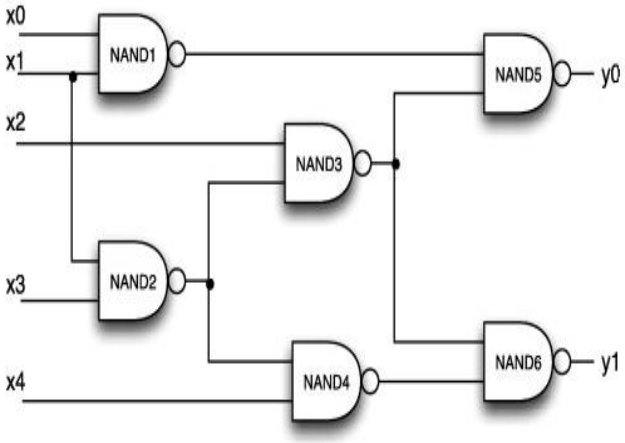

Fig 4.3 C17 bench mark circuit

V. RESULTS

5.1 RTL SCHEMATIC:

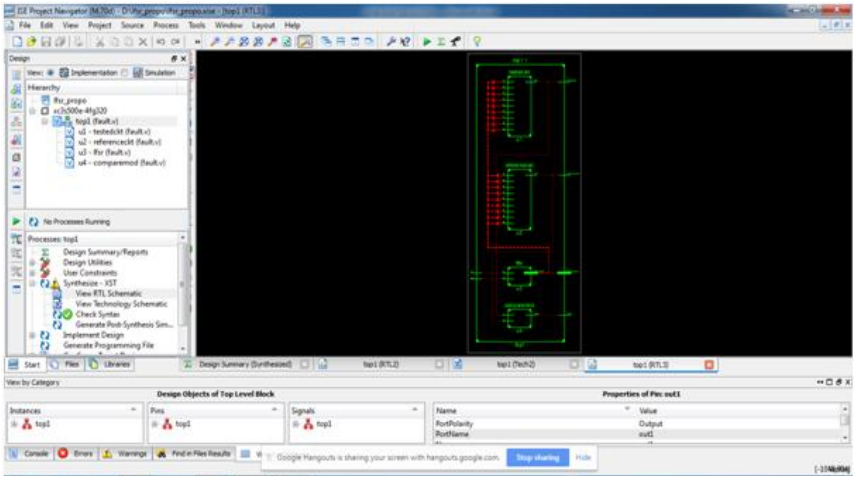

Fig:5.1RTL Schematic

RTL schematic gives the information about the user view of the design

5.2Technology Schematic:

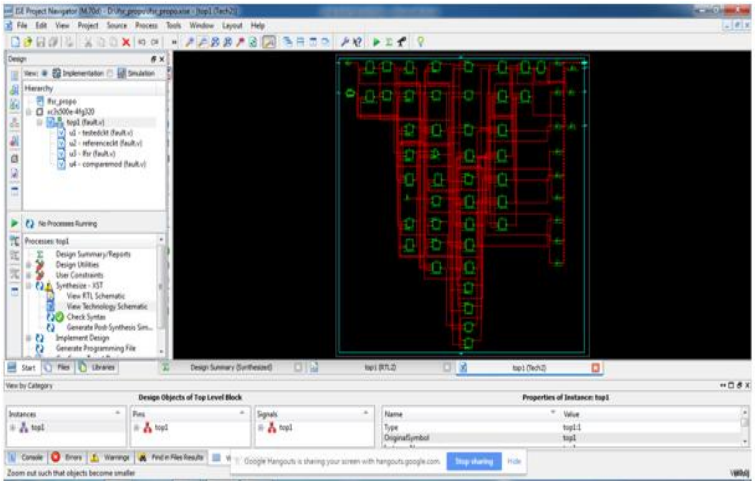

Fig 5.2 Technology Schematic

Technology schematic gives the information about the chip view of the design

5.2 Waveform:

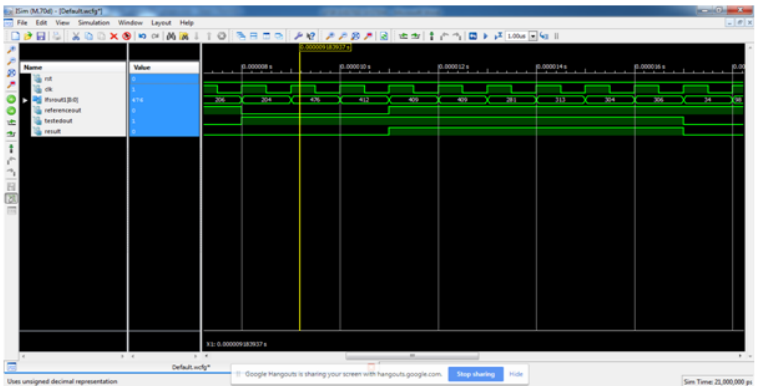

Fig 5.3 Waveform

In the above waveform clk , reset are the inputs which are applied to the system. Whereas lfsrout is the output of the system. Whenever the clk is at the positive edge triggered then only the transaction will happen. If both the reference out and tested out signal are equal then the circuit is fault less otherwise the circuit is in fault state. This waveform also indicates the fault coverage of the system along with test pattern generation.

VI. CONCLUSION

In this paper the proposed method showing how the test patters are generated with more correlation which misses in the existed one. Based on the simulation results it will understand how the circuit is determining the fault coverage. In the proposed system the number of LUT's (look up tables) 23 consumes less area when compare with the existing system 27. Obviously the power consumption is also less in the proposed design which is 0.18mw when compare with the existing 0.22mw. By doing changes in the proposed architecture there is a chance of further reduction in the power consumption in the near future. In this paper VERILOG is used for implementing the RTL. XILINX ISE 12.3i is used for performing synthesis.

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