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New Topology for 13-Level Inverter and THD Calculation by using Different PWM Strategies

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Abstract-In recent years construction of multilevel inverters are extremely getting used for moderate voltage and extreme power applications due to their benefits corresponding to low voltage stress on the ability switches, low dv/dt magnitude relation to produce lower harmonic contents within the output voltage and current. Multilevel inverters are disadvantages of increasing levels because of using more number of switches. It may be produces switching losses, complex circuitry. The planned formation contains less switches so produce less switching losses and lesser harmonics within the output voltage than the standard electrical converter topologies. The modulation technique used in this paper is level shifted. To generating the gating signals, to limit the frequency and harmonics of the output voltage wave form of the inverter, the sinusoidal PWM method has been applied to the power switches. PWM techniques are used in this paper are In Phase Disposition PWM, Alternative Opposition Disposition PWM, Carrier Overlap PWM, Variable Frequency PWM techniques. The results are valid through the harmonic spectrum of the field-effect transistor window by exploitation MATLAB/SIMULINK.

Keywords- Sinusoidal Pulse Width Modulation- SPWM, Multilevel Level Inverter-(MLI), Total Harmonic Distortion-THD (%), Filter**.**

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I. INTRODUCTION

Power electronic schemes play a vital role inside the conversion and executive of electric power, significantly to extract power from renewable energy sources like electrical phenomenon array and wind energy. Multilevel electrical inverter topologies are Diode clamped [1], Flying condenser [2], Cascaded H-bridge inverter are the 3 main totally different types of inverter structures that are utilized in industrial applications. In flying condenser and diode clamped inverter there's a retardant of capacitance voltage equalization, and this drawback is overcome in cascaded H-bridge inverter. In cascaded H-bridge once levels are increasing it needs additional range of semiconductor switches, thus complexness can increase and high cost also[3].Conversion of DC to AC power will be finished the assistance of inverters (single phase section or 3 phase section) by different Switching patterns. But they need associate additionally creates harmonics in output voltage and we need to use filter it. So we have a tendency to use SPWM sinusoidal Pulse width Modulation inverter which provides AC output including harmonics at switching state of upper frequency then it. So it's simply filtered by using little low pass filter LC that is compact with reference to different inverter filters [4].Conventional bipolar inverters turn out alternating step waveforms with higher harmonics. Thus, the structure inverters (MLI) were developed .This paper provides a newly discovered 3 phase configuration to provide the I3-level output with Minimum total harmonic distortion (THD) in its output voltage. IPD, APD, CO and VF PWM techniques were wont to produce switching pulses [6]-[7]-[8].Conventional bipolar inverters were the diode clamped MLI has twenty four switches per section to provide a 13 level staircase waveform as the output voltage. The capacitance clamped MLI uses twenty four switches per section whereas the cascaded H-bridge electrical converter uses twenty four switches per part to produce an identical output.This paper reports a single phase inverter configuration with ten switches and 4 DC sources. 3 phase multilevel inverter is obtained by interconnecting three single phase inverters to a star connected pure resistive load with a standard earth Point. Therefore, this circuit offers lesser gate control electronic equipment, lesser price, lesser heating, and ease of installation and lesser magnetism interference.

II. MULTILEVEL SPWM INVERTER

Multilevel inverters generates a staircase waveform in multiple steps of output that reduces the output THD. As we have a tendency to increase the number of step levels in multilevel inverter we tendency to receive a lot of sinusoidal output and harmonic distortion reduced as per level of inverter will increase. We also reduce higher level harmonics and increase output voltage RMS exploitation by SPWM inverter. Smoothness of wave is increases when voltage levels increases. To regulate the frequency and harmonics of the output voltage of the inverter, we have an inclination to should select the foremost acceptable PWM technique.The curving PWM (SPWM) technique has been applied to the ability switches, during that a reference sinusoidal wave of basic is compared to high frequency carrier waves.The modulation indices are kept same in all the strategies for comparison.This paper is categorize into several sections. Section I contains the circuit configuration and its modes of operation. Section II contains some pulse width modulation schemes (indices) accessible for switching of the inverter. The simulation outcomes are analyzed in section III. The wave shape obtained once to apply the series LC filter at the inverter output. It is analyzed in section IV. V segment provides the conclusion.

Table .1 Calculation Of number of voltage sources Used for Different Levels of Inverters.

LEVEL $(\mathbf{N_{Level}})$	**NUMBER OF VOLTAGE SOURCES REQUIRED (S)**
$\mathbf{N_{LEVEL=2S+1}}$	$\mathbf{S=\frac{N_{LEVEL-1}}{2}}$
9	4
11	5
13	6
15	7

I-Proposed Method And Its Opertation

The proposed inverter method has ten switches and four sources per phase as shown in fig1. The series combination of the DC sources are Vdc, Vdc, 2Vdc, 2Vdc are often used to manufacture 13 level inverter output during a single cycle. In each mode, five of the switches operates.The planned topology is easy in design and compared to the present topologies, it consists of 4 DC sources and ten switches. It even have additional options like only five switches conducting at an interval of time.

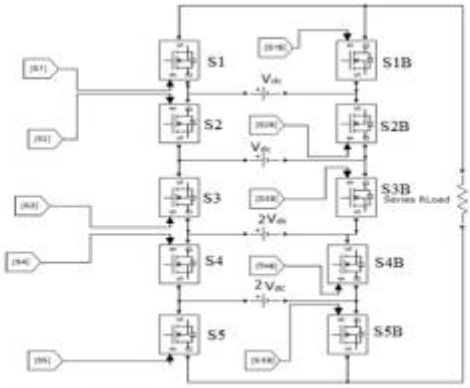

Fig.1.Proposed Configuration for Single Phase Inverter Operation

The general formula for the number of switches and also the number of dc sources for the planned topology is given byN= (2*S+1)(N=number of levels,S=number of dc voltage sources). Here we using 4 voltage sources are Vdc, Vdc, 2Vdc, and 2Vdc totally here we using 6 Vdc sources.

Ii.Amplitude Modulation Indices

$$m_a = \frac{\text{amplitude of the referencewave}}{\text{amplitude of the carrierwave}}$$

$$m_f = \frac{\text{frequency of the carrierwave}}{\text{frequency of the modulatingwave}}$$

The amplitude modulation index maintained at 0.9 and also the FM index at 200. The RMS worth of the fundamental component of the output voltage and also the total harmonic distortion (THD) area unit discovered by victimization simulation results.

Conducting Staes Of 13 Level Inverter

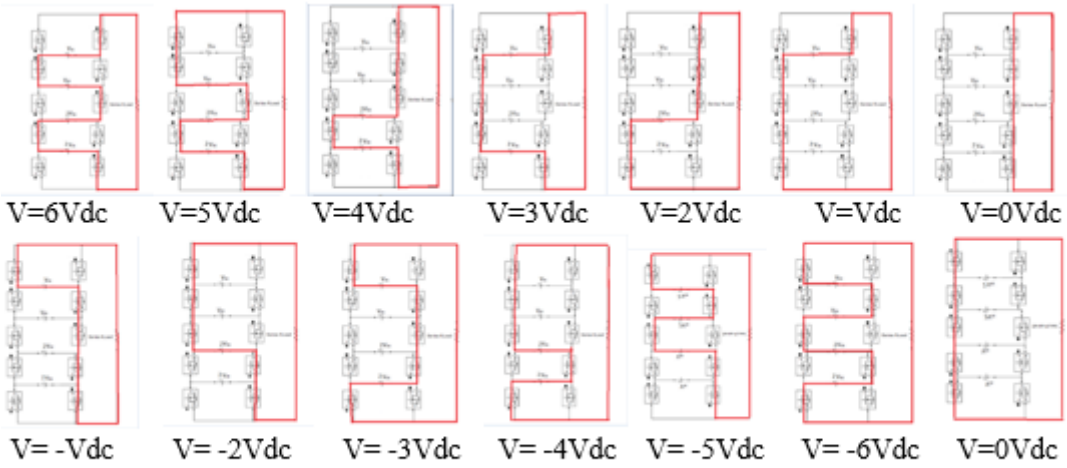

Fig.2 shows the conducting switches at different operating switching states (Each Output Level).

+V_{dc}Level voltage is obtained by turning on the switches S2, S3, S4, S5, and S1B together. And also -$2V_{dc}$ obtained by turning on the switches S1, S2, S3, S3B, S4B.Similarly, all the DC output voltage levels are obtained.

2.1 IPD-LSPWM (In Phase Disposition Level Shift PWM)

In this method we use constant amplitude is l V and a frequency of 10 kHz. The extent (level) shifted carrier signals are compared with a same fundamental sine wave. The dissimilar levels of the output wave is observed and decoded to produce the pulses needed to trigger every switch within the inverter.

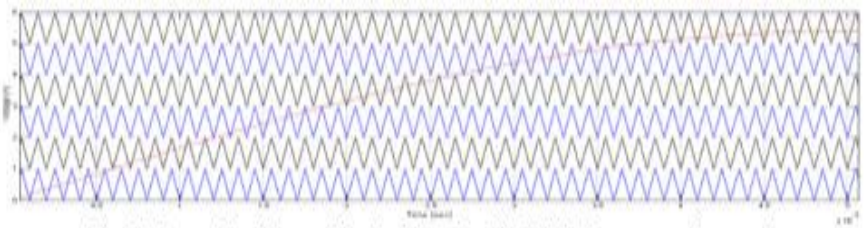

Fig.3.Reference Sine Wave and Carrier Waves for IPD-LSPWM at $m_{a=0.9}$ and $m_{f=200}$

2.2 APD-LSPWM (Anti Phase Disposition Level Shift PWM)

Each carrier signal is out of phase with nearby carrier signals by 180° and have constant amplitude and frequency. The carrier signals are compared with the reference wave (which is at fundamental frequency) to provide required gate pulses.

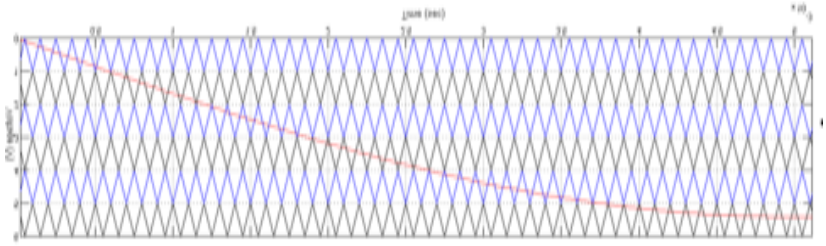

Fig.4.Reference Sine Wave and Carrier Waves for APD-LSPWM at$m_{a=0.9}$ and $m_{f=200}$

2.3 **CO-LSPWM (**Carrier Overlap Level Shift PWM**)**

This method applicable level shifted carrier waves of the same frequency and amplitude. They are in phase with each and every signal and conjointly overlap one another. They're compared to a diode bridge corrected reference wave so as to produce the gate pulses. And that all compared with same reference sine wave to get gating signals of various switches of inverters.

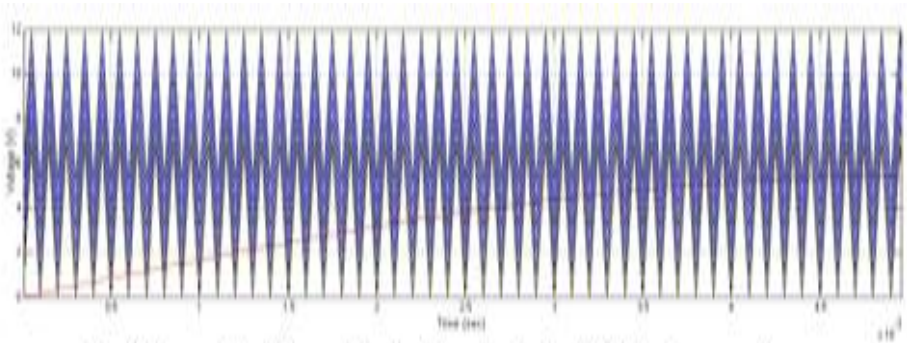

Fig.5 Reference Sine Wave and Carrier Waves for Carrier-LSPWM at $m_{a=0.9}$ and $m_{f=200}$

2.4VF-LSPWM (Variable Frequency Level Shift PWM)

All the level-shifted carrier waves have a similar amplitude. The nethermost (lower) carrier has very high frequency, 10 kHz followed by 8 kHz, 6 kHz, and 4 kHz and also the uppermost carrier signal has lowest frequency 2 kHz. They are compared with the reference sine wave with fundamental frequency to provide required switch pulses.

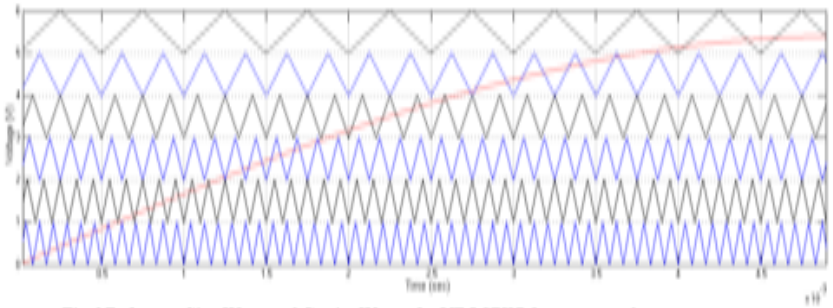

Fig.6 Reference Sine Wave and Carrier Waves for VF-LSPWM at $m_{a=0.9}$ and $m_{f=200}$

Iii.Simulink Results &Discussion

Various PWM techniques are applied to the planned three phase inverter topology at constant amplitude and frequency modulation indices exploitation by MATLAB/ SIMULINK.

The circuit parameters are Amplitude Modulation (A_m) =4.5V, Frequency Modulation (f_m) =50KHZ, Amplitude Frequency (A_f) = 5V, Carrier Frequency (f_c) = 10KH, Star Connected Resistance Load =50Ω.

3.1 IPD-LSPWM OUTPUT WAVEFORM

The three phase output voltage waveform obtained from IPD-LSPWM method is shown in Fig.7. It has to significant of 3^{th},5^{th},11^{th}, 15^{th} and 19^{th} harmonic values as given by its FET analysis in fig.8. The carrier waves are in phase with one another basic wave of the IPD type, leading to less complicated circuitry.

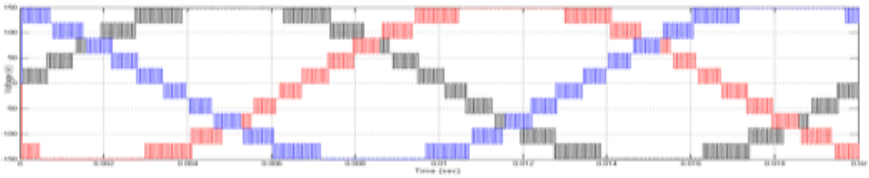

Fig.7.Output voltage waveform for the three phase 13 level Inverter using IPD-LSPWM method

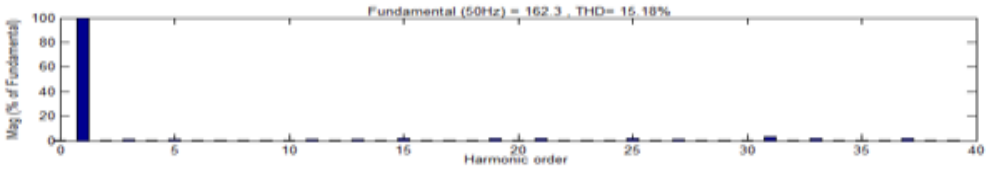

Fig.8.FET Analysis of the harmonic spectrum for IPD-LSPWM method

3.2 APD-LSPWM OUTPUT WAVEFORM

The output voltage waveform and the FET analysis of THD for APD-LSPWM technique are shown in fig.9and fig.10 respectively. The3^{th},5^{th},11^{th},13^{th},15^{th},19^{th},21^{th},25^{th}and19^{th},21^{th},25^{th},and33^{th}harmonics are significant.They produce RMS value more than the IPD-LSPWM method, THD lesser than IPD-LSPWM. The carrier waves are anti-phase with each other wave form.

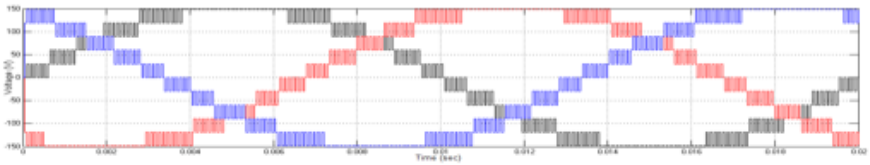

Fig.9.Output voltage waveform for the three phase13 level Inverter using APD-LSPWM method

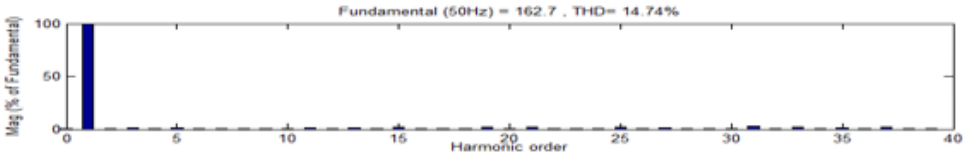

Fig.10.FET Analysis of the harmonic spectrum for APD-LSPWM method

3.3 CO-LSPWM OUTPUT WAVEFORM

Fig.11 Provides the FET analysis of the output voltage of CO-PWM method is shown in fig.12.The 3^{th},5^{th},9^{th},11^{th},15^{th},19^{th},21^{th},25^{th}and33^{th}harmonics have higher energy.The output produced by C0-PWM has highest THD of 100.70% and lowest RMS value of fundamental output voltage of 90.87V among the four methods.This method produces pulses that overlap each other. Hence, the subsequent voltage waveform has very high value of Total Harmonic Distortion.

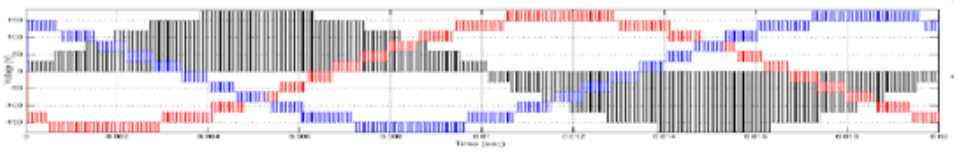

Fig.11.Output voltage waveform for the three phase13 level Inverter using CO-LSPWM Method

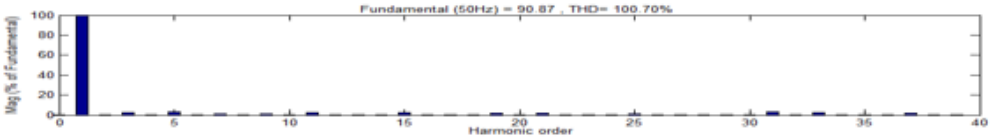

Fig.12.FET Analysis of the harmonic spectrum for CO-LSPWM Method.

3.4 VF-LSPWM OUTPUT WAVEFORM

The FET of the inverter output voltage in fig.13. From the VF-PWM method is demonstrated in fig.14. The THD obtained through this method is (different frequencies used) only 10.86%. The spectrum has morein2^{th}, 3^{th}, 4^{th}, 6^{th} and 7^{th} harmonic energy. VF-PWM technique was produce minimum harmonics in the output voltage wave form among four types.

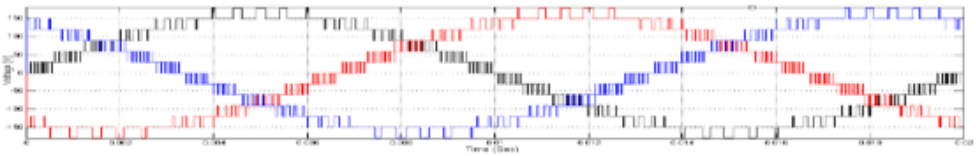

Fig.13.Output voltage waveform for the three phase13 level inverter using VF-LSPWM Method

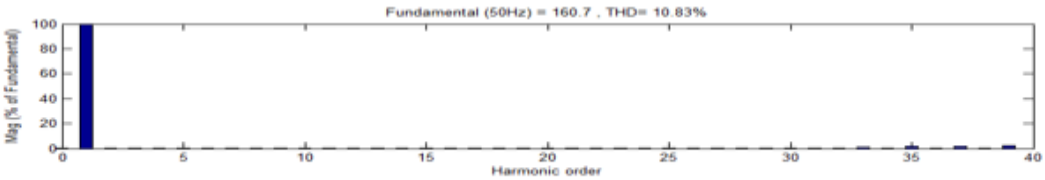

Fig.14.FET Analysis of the harmonic spectrum for VF-LSPWM Method.

Table.2. Different Pulse Width Modulation Methods of Output Voltages and THD Values

SL.N0.	PWM Technique	RMS Value Of Fundamental Of Output Voltage (in voltage)	THD (in %)
1	IPD-LSPWM	162.3	15.18
2	APD-LSPWM	162.7	14.74
3	CO-PWM	90.87	100.70
4	VF-PWM	160.7	10.83

IV. Wave Form For After Using LC-Filter

An L-C filter is connected at the output of the inverter to produce a sinusoidal curved wave with reduced THD. The L and C values are$L \geq \frac{R_{L-max}}{3\omega}$(for single phase), $L \geq 2* \frac{R_{L-max}}{3\omega}$(for poly phase)
(Where P is Number of Phases and$\omega = 2\Pi f$)

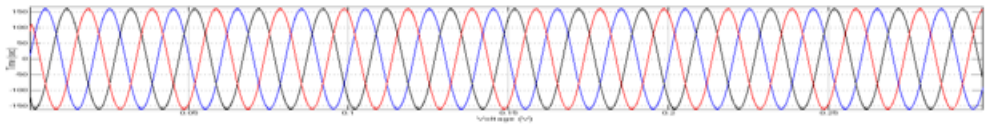

Fig. 15.Output voltage waveform for the three phase 13 level Inverter using VF-LSPWM method after LC filter.

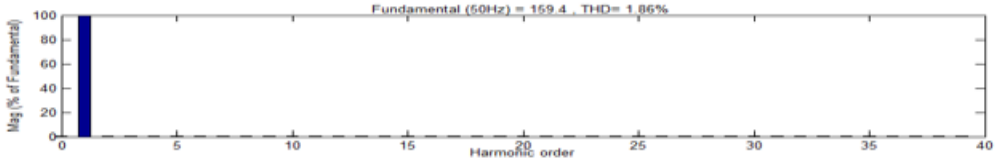

Fig. 16.FET Analysis of the harmonic spectrum for VF-LSPWM Method after LC filter.

The three phase Ten Switched Type Multilevel Inverter is connected to a star, connected to a pure load resistance of 50Ω. The capacitance value of the filter is assumed as 1μF.
The signal obtained after the LC filter exhibits 1.86% THD inFig.15.The details of the harmonics of the output AC voltage waveform in fig. 16.

III. CONCLUSION

Three phase thirteen level inverter topology with compact number of switches proposed and simulated. Various PWM techniques are fabricated and compared. From the simulated results, variable

pwm technique (VF-PWM) exhibits less THD of 10.86% in the inverter production voltage waveform. Variable frequency method the best PWM technique for inverter switching because compact (small) can be used in the LC filter placed in series to the inverter output to produce a 13 level AC sine wave of less THD as shown in Fig.16. It produces least THD of 1.86%.

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